HPCG on Intel Architecture Update
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Intel Corporation

SC15, HPCG BoF
Outline

• IA result updates
• Our other work related to HPCG
• HPCG 3.0 optimizations
## Single-Node Results in IA

<table>
<thead>
<tr>
<th>System</th>
<th>Single-node Perf. (GFLOP/s)</th>
<th>Efficiency w.r.t. STREAM</th>
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<td>2-skt 14c Xeon E5-2697 v3 @ 2.6 GHz (HSW)¹</td>
<td>18.4</td>
<td>104%</td>
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¹ Results from JHPC paper. STREAM BW 108 GB/s is used for BW efficiency. 1 MPI rank per socket, 14 threads per rank (1 thread per core), KMP_AFFINITY=granularity=fine,compact,1, lexicographical GS at all MG levels, 50 CG iterations

² Results from JHPC paper. STREAM BW 170 GB/s is used for BW efficiency, 12 MPI ranks, 20 threads per rank (4 threads per core), KMP_AFFINITY=granularity=fine,compact, lexicographical GS at top 2 MG levels, multi-color GS at the other levels. 51 CG iterations
**Single-Node Results in IA**

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1) Results from JHPC paper. STREAM BW 108 GB/s is used for BW efficiency. 1 MPI rank per socket, 14 threads.

Newer Xeon processors have higher efficiency w.r.t. STREAM BW.

2) Results from JHPC paper. STREAM BW 170 GB/s is used for BW efficiency, 12 MPI ranks, 20 threads per rank (4 threads per core), KMP_AFFINITY=granularity=fine,compact, lexicographical GS at top 2 MG levels, multi-color GS at the other levels. 51 CG iterations.
## Multi-Node Results in IA

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1) Results from ISC14. STREAM BW 150 GB/s per Intel® Xeon Phi™ coprocessors. Intel® Xeon® processors were not used for computation, and their STREAM BW was excluded when computing BW efficiency.
2) STREAM BW 110 GB/s per node is used for BW efficiency.
3) Both Xeon processors and Xeon Phi coprocessors are used. 80 GB/s Xeon processor STREAM BW and 170 GB/s Xeon Phi coprocessor STREAM BW is used for BW efficiency.
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**Stampede result is from only 2/3 of the full cluster. Stampede has similar per node performance to GPU clusters.**
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Work related to HPCG (1)

MKL 11.3 inspector-executor sparse BLAS routines

- Sparse matrix-vector multiplication (SpMV)
- Sparse triangular solver (SpTS)
- Sparse matrix-matrix multiplication (SpGEMM)
- ...

Work related to HPCG (2)

SpMP: Open-source library for optimized sparse matrix pre-processing

- [https://github.com/jspark1105/SpMP](https://github.com/jspark1105/SpMP)
- Task dependency graph construction, BFS/RCM reordering, ...
- Can be useful for libraries implementing their own SpTS, ILU, ...
- Helped a customer wanted optimized ILU preconditioners
Work related to HPCG (3)

Optimizing algebraic multi-grid implementation in HYPRE library

- High-Performance Algebraic Multigrid Solver Optimized for Multi-Core Based Distributed Parallel Systems, Park et al., SC15

- Common optimizations: efficient lexicographical GS, matrix reordering for cache locality optimization, ...
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HPCG 3.0 Optimizations in newly timed routines, GenerateProblem and SetupHalo

Separate interior and boundary points

- Handling interior points (common case) is easily parallelized

Halo setup with boundary points

- **Thread-private std::unordered_map**
  (most duplicates eliminated here due to locality)
- Concatenate thread private maps into an array
- **std::sort and std::unique**

Similar patterns in HYPRE AMG library
HPCG 3.0 on HSW

Setups are the same as in “Optimizations in High-Performance Conjugate Gradient Benchmark for IA-based Multi and Many-core Processors” in JHPC, Table II used for single node experiments.
HPCG 3.0 on HSW

Overhead reduced to <3%
HPCG 3.0 on Knights Corner

Setups are the same as in “Optimizations in High-Performance Conjugate Gradient Benchmark for IA-based Multi and Many-core Processors” in JHPC, Table II used for single node experiments.
HPCG 3.0 on Knights Corner

Overhead reduced to <4%
Baseline: more ranks $\rightarrow$ smaller overhead (no omp par.)
Optimized: more ranks $\rightarrow$ more overhead (more boundaries)
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