HPCG on Intel Xeon Phi 2nd Generation, Knights Landing

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Outline

• KNL results

• Our other work related to HPCG
November 2016 HPCG Results

<table>
<thead>
<tr>
<th>Rank</th>
<th>Site</th>
<th>Computer</th>
<th>Cores</th>
<th>HPL Rank (Pflops)</th>
<th>TOP500 Rank</th>
<th>HPCG (Pflops)</th>
<th>Fraction of Peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RIKEN Advanced Institute for Computational Science Japan</td>
<td>K computer – SPARC64 VIII fx 2.0GHz, Tofu interconnect</td>
<td>705,024</td>
<td>10.510</td>
<td>7</td>
<td>0.6027</td>
<td>5.3%</td>
</tr>
<tr>
<td>2</td>
<td>NSCC / Guangzhou China</td>
<td>Tianhe-2 (MilkyWay-2) – TH-IVB-FEP Cluster, Intel Xeon 12C 2.2GHz, TH Express 2, Intel Xeon Phi 31S1P 57-core NUDT</td>
<td>3,120,000</td>
<td>33.863</td>
<td>2</td>
<td>0.5800</td>
<td>1.1%</td>
</tr>
<tr>
<td>3</td>
<td>Joint Center for Advanced High Performance Computing Japan</td>
<td>Oakforest-PACS – PRIMERGY CX600 M1, Intel Xeon Phi Processor 7250 68C 1.4GHz, Intel Omni-Path Architecture</td>
<td>557,056</td>
<td>13.555</td>
<td>6</td>
<td>0.3855</td>
<td>1.5%</td>
</tr>
<tr>
<td>4</td>
<td>National Supercomputing Center in Wuxi China</td>
<td>Sunway TaihuLight – Sunway MPP, SW26010 260C 1.45GHz, Sunway NRCP</td>
<td>10,649,600</td>
<td>93.015</td>
<td>1</td>
<td>0.3712</td>
<td>0.3%</td>
</tr>
<tr>
<td>5</td>
<td>DOE/SC/LBNL/NERSC USA</td>
<td>Cori – XC40, Intel Xeon Phi 7250 68C 1.4GHz, Cray Aries Cray</td>
<td>632,400</td>
<td>13.832</td>
<td>5</td>
<td>0.3554</td>
<td>1.3%</td>
</tr>
<tr>
<td>6</td>
<td>DOE/NNSA/LLNL USA</td>
<td>Sequoia – IBM BlueGene/Q, PowerPC A2 1.6 GHz 16-core, 5D Torus IBM</td>
<td>1,572,864</td>
<td>17.173</td>
<td>4</td>
<td>0.3304</td>
<td>1.6%</td>
</tr>
<tr>
<td>7</td>
<td>DOE/SC/Oak Ridge Nat Lab USA</td>
<td>Titan – Cray XK7, Opteron 6274 16C 2.200GHz, Cray Gemini interconnect, NVIDIA K20x Cray</td>
<td>560,640</td>
<td>17.590</td>
<td>3</td>
<td>0.3223</td>
<td>1.2%</td>
</tr>
<tr>
<td>8</td>
<td>DOE/NNSA/LANL/SNL USA</td>
<td>Trinity – Cray XC40, Intel Xeon E5-2698 V3, Aries custom Cray</td>
<td>301,056</td>
<td>8.101</td>
<td>10</td>
<td>0.1826</td>
<td>1.6%</td>
</tr>
<tr>
<td>9</td>
<td>NASA / Mountain View USA</td>
<td>Pleiades – SGI ICE X, Intel Xeon E5-2670, E5-2680V2, E5-2680V3, E5-2680V4, Infiniband FDR HPE/SGI</td>
<td>243,008</td>
<td>5.952</td>
<td>13</td>
<td>0.1752</td>
<td>2.5%</td>
</tr>
<tr>
<td>10</td>
<td>DOE/SC/Argonne National Laboratory USA</td>
<td>Mira – IBM BlueGene/Q, PowerPC A2 1.6 GHz 16-core, 5D Torus IBM</td>
<td>786,432</td>
<td>8.587</td>
<td>9</td>
<td>0.1670</td>
<td>1.7%</td>
</tr>
</tbody>
</table>

~47 GF/s per KNL

~10 GF/s per HSW
Single-Node KNL

<table>
<thead>
<tr>
<th></th>
<th>Perf. (GFLOP/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>72c Xeon Phi 7290</td>
<td>51.3 (flat mode)</td>
</tr>
<tr>
<td>68c Xeon Phi 7250</td>
<td>49.4 (flat mode), 13.8 (DDR)</td>
</tr>
<tr>
<td>64c Xeon Phi 7210</td>
<td>46.7 (flat mode)</td>
</tr>
</tbody>
</table>

Cache mode provides a similar performance (~3% drop)
MCDRAM provides >3.5x performance than DDR
Easier to use than KNC
Less reliance on software prefetching
2 threads per core is enough to get the best performance
Smaller gap between SpMV using CSR and SELLPACK for U of Florida Matrix Collection

n=192 usually gives the best results. All results are measured with quad cluster mode and code from https://software.intel.com/en-us/articles/intel-mkl-benchmarks-suite
Multi-Node KNL

Each node in flat/quad mode connected with Omni-Path fabric (OPA)
Outline

• IA result updates
• Our other work related to HPCG
Related Work (1) – Library

MKL inspector-executor sparse BLAS routines

SpMP open source library (https://github.com/jspark1105/SpMP)
BFS/RCM reordering, task graph construction of SpTrSv and ILU, ...

Optimizing AMG in HYPRE library
Included from HYPRE 2.11.0
Related Work (2) – Compiler

Automating Wavefront Parallelization for Sparse Matrix Computations, Venkat et al., SC’16

Fig. 8. Speedup of Parallel PCG over Sequential PCG.

12-core Xeon E5-2695 v2, ILU0 pre-conditioner, speedups include inspection overhead time
Related Work (3) – Script Language

Sparso: Context-driven Optimizations of Sparse Linear Algebra, Rong et al., PACT’16, https://github.com/IntelLabs/Sparso

14-core Xeon E5-2697 v3, Julia with Sparso package
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